**Chapter 17 - Exercises**

17.1 List and briefly define three types of computer system organization.

**List and briefly define three types of computer system organization.  
Single instruction, single data (SISD) stream architecture:  
The control unit (CU) of the processing unit (PU) will execute a single instruction stream (IS) in order to perform the operations on the data stored in a single memory unit (MU).  
  
Single instruction, multiple data (SIMD) stream architecture:  
A single machine instruction can control the execution of multiple processing elements simultaneously.  
  
Multiple instructions, multiple data (MIMD) stream architecture:  
A set of processors executing different set of instruction sequences on different data sets simultaneously**

17.2 What are the chief characteristics of an SMP (symmetric multiprocessor)?

**• There are two or more processors that are having equal capabilities  
• These processors are sharing the same main memory and Input-Output (I/O) devices.  
• These processors are interconnected with a system bus so that the access time of memory is same for every processor.  
• All processors can have access to I/O devices whether it may be through same path or other.  
• As it is a parallel processing technique a function can be done by all the multiprocessors parallel.  
• The Operating System presents in the system controls the system and provides interaction between processors and their jobs.  
• The Operating System of an SMP is responsible for scheduling the processes or threads across all processors.**

17.3 What are some of the potential advantages of an SMP compared with a uniprocessor?

**● Performance  
● Avalablity  
● Incremental growth  
● Scaling**

17.4 What are some of the key OS design issues for an SMP?

**● Simultaneous concurrent processes  
● Scheduling  
● Synchronization  
● Memory management  
● Reliability and fault tolerance**

17.5 What is the difference between software and hardware cache coherent schemes?

**This is a means of ensuring consistency in Caching. This is a big concern in a multicore environment due to the presence of distributed L1 and L2 caches. The problem here is that each core maintains its own cache, and the copy of data in a given core's cache may sometimes not be the latest version, and this poses the problem of data inconsistency.**

**There are essentially two mechanisms for ensuring Cache coherence. These mechanisms are what is known as Cache Coherence Schemes.**

**Software Cache Coherent Scheme**

**Software cache coherence schemes attempt to avoid the need for additional hardware circuitry and logic by relying on the compiler and operating system to deal with the problem. All the rules for ensuring cache coherence is embedded in a software code.**

**Hardware Cache Coherence Scheme  
  
In hardware schemes, the cache coherence logic is implemented in hardware. The hardware has encoded in it all the needed data localities and caching strategies. There is minimal need for additional software code or instructions as the embedded system logic controller handles that already.**

17.6 What is the meaning of each of the four states in the MESI protocol?

**Here's what MESI stands for**

**Modified: The line in the cache has been modified (different from main memory) and is available only in this cache.**

**Exclusive: The line in the cache is the same as that in main memory and is not present in any other cache.**

**Shared: The line in the cache is the same as that in main memory and may be present in another cache.**

**Invalid: The line in the cache does not contain valid data.**

**Answers to Questions**